REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-6, and 10-26 are now in the application. Claim 1 has been amended. Claims 7-9 have been canceled. Claims 14-26 have been added.

Support for the amendments in the claims may be found as follows:

Claim 1 now combines the original claim 1 and the subject matter of claim 7. Moreover, we have clarified that the capacitor is an electrical capacitor (see, page 8, second paragraph). Moreover, in accordance with the disclosure of the PCT application, on which the present application is based, we have defined that an increase of the variable is effected in response to the execution of an operation.

New independent **claim 14** defines that the processor comprises a clock generator, that the clock generator is adapted such that the greater the charge of the electrical capacitor is, the lower is the frequency of the clock signal generated by the clock generator and that the frequency of the clock signal influences the speed of the computation unit (see, page 8, third paragraph, and page 9, first paragraph).

New independent **claim 15** is based on pending independent claim 1 and further comprises the subject matter of claims 8 and 9.

New dependent **claim 16** further defines that the speed of the computation is controlled in response to a difference signal representing a difference between the first temperature and the second temperature (see, page 12, first paragraph).

New dependent **claim 17** defines that the processor comprises a first temperature sensor adapted to determine the first temperature and a second temperature sensor adapted to determine the second temperature, wherein the first temperature sensor and the second temperature sensor are located in different places of the thermal capacitance (see, page 12, first and second paragraphs).

New dependent **claim 18** defines that the first temperature sensor and the second temperature sensor are located at two places of the computation unit which warm up to different extents or at different rates on execution of an operation by the computation unit (see, page 12, second paragraph).

New dependent **claim 19** defines that the processor is adapted such that the difference between the first temperature and the second temperature results in a reduction of the speed of the computation unit (see, page 12, third paragraph and page 13, first paragraph).

New independent **claim 20** is based or original independent claim 1 and further comprises the subject matter of claim 8. Further, we have defined that the processor comprises an electrical filament resistor adapted to supply energy to the thermal capacitance in response to the execution of an operation in the computation unit (see, page 11, second paragraph).

New independent **claim 21** is based on claim 1 and further defines that the processor comprises a clock generator (see, page 10, second paragraph). Moreover, new independent claim 21 comprises the subject matter of pending dependent claim 8. Besides, new independent claim 21 defines that the state unit comprises a temperature sensor (see, page 10, second paragraph), that the clock generator is adapted such that an output signal of the temperature sensor controls a clock rate generated by the clock generator (see, page 10, second paragraph) and that the clock rate generated in the clock generator controls the speed of the computation unit (see, page 10, second paragraph and page 11, first paragraph).

New independent **claim 22** is based on claim 1 and further summarizes the subject matter of claims 5 and 6.

New independent **claim 23** is based on pending independent claim 1 and further defines that the processor is adapted to change the speed of the computation unit in steps in dependence on in the state of the state unit, to set the speed of the computation unit to a first high speed or to a second lower speed (see, page 14, fourth paragraph and page 15, first paragraph).

New independent **claim 24** is based on claim 1 and further defines that the processor is adapted to allow for setting a factor for a relationship between a state of the state unit and the speed of the calculation unit or for setting an amount of energy supplied to the state unit by means of a programmable parameter (see, page 16, first paragraph).

New independent **claim 25** is based on claim 1 and further comprises the subject matter of claim 11.

New independent **claim 26** is based on claim 1 and further defines that wait clock intervals are introduced to decrease the speed of the calculation unit (see, page 14, second paragraph).

Double Patenting

We have carefully reviewed the nonstatutory obviousness-type double patenting rejection in paragraph 5. We respectfully request reconsideration on the grounds that the currently presented claims are patentably distinct from the claims of the commonly assigned U.S. Patent No. US 6,999,333 B2.

The subject matter claimed in US 6,999,333 B2 is substantially different from the subject matter claimed within the present application. While US 6,999,333 pertains to a method and apparatus for assessing one-time programmable cells of a memory, the present application is concerned with the adjustment of the speed of operation of a computation unit. For this reason we respectfully disagree that it would be obvious "that controlling the speed of a computation unit is equivalent to indicating an uncertain programming state" (see, section 3 of the Office Action).

It should be noted here the concept of operating on programmable memory cells to assess the electric characteristics thereof has nothing in common with adjusting the

speed of a computation unit. It follows that US 6,999,333 and the claims of the present application protect entirely distinct subject matter.

At this time, a terminal disclaimer is not deemed necessary. The Examiner is respectfully requested to reconsider the provisional rejection.

Claim Rejections – 35 U.S.C. § 102

We now turn to the art rejection in which the claims, as presented on Dec. 27, 2004 have been rejected as being anticipated by Curiger et al. (US 6,330,668, hereinafter "Curiger") under 35 U.S.C. § 102(e). We respectfully traverse on the basis of the amended claims. The Examiner is requested to consider the following.

Curiger deals with providing timing and clock signals to an encryption calculation circuitry making use of an on-chip-oscillator (see, column 4, lines 42-55). Moreover, the reference describes that temperature impacts the frequency of the on chip oscillator wherein the frequency of the on chip oscillator increases as the temperature decreases.

Curiger does not mention an electrical capacitor, the charge of which is increased in response to the execution of an operation by the computation unit, wherein the speed of the computation unit is decreased in response to an increase of the charge of the capacitor. Thus, the subject matter of the new independent claim 1 should be considered to be novel over the teachings of Curiger.

The same argument holds for the subject matter of new independent claim 11.

Regarding new independent claim 15, Curiger describes that the frequency of the on chip oscillator is dependent on the temperature of the chip. In contrast, new independent claim 15 defines that two temperatures are evaluated in order to determine the speed of the computation unit. Assessing two different temperatures is not shown in Curiger. Thus, the subject matter of new independent claim 15 should be considered to be novel over the disclosure of Curiger. Moreover, additional specific features have been defined in the new dependent claims 16-19.

Curiger is entirely silent with regard to evaluating two different temperatures or even a difference between two temperatures. Thus, the subject matter of new dependent claim 16 is clearly novel.

Also, Curiger does not describe the presence of two temperature sensors located at different places of a thermal capacitance, wherein the speed of the computation unit is controlled independence on the signals from the two temperature sensors located at different places of the thermal capacitance. Thus, the subject matter of the new dependent claim 17 is novel.

Curiger does not even mention a single temperature sensor and does not anticipate the presence of two temperature sensors which are arranged in a specific way, as defined by new dependent claim 18. Thus, the subject matter of new dependent claim 18 should also be considered allowable.

Moreover, as Curiger does not mention evaluating the difference between two temperatures, the subject matter of the new dependent claim 19 should be considered to be allowable.

Regarding the new independent claim 20, it should be noted that Curiger does not teach to introduce into the chip an electrical filament resistor. Also, Curiger does not disclose operating any resistor in response to the execution of an operation in the computation unit. Thus, the subject matter of the new independent claim 20 should be considered to be allowable.

Regarding new independent claim 21, it should be noted that Curiger is silent about a temperature sensor which provides an output signal to a clock rate generator, wherein the output signal of the temperature sensor controls the clock rate generated by the clock generator. In contrast, Curiger does not disclose any temperature sensor. Curiger merely discloses a ring oscillator, which does not comprise a temperature sensor. In contrast, a ring oscillator merely comprises a plurality of transistors which form a feed back loop of CMOS inverters. Thus, the presence of a temperature sensor is neither explicitly described in Curiger nor implied by the disclosure of Curiger. Consequently, the subject matter of independent claim 18 should be considered to be allowable in view of Curiger.

Regarding new independent claim 22, Curiger does not disclose any specific dependence of the speed of the computation unit from any state variable. Curiger merely defines that the temperature impacts the preferred oscillation circuit in much the same way it impacts CMOS silicon circuitry in general (see, column 4, lines 58-

60). Moreover, Curiger describes that the on chip oscillator will increase its output frequency if the temperature decreases. In contrast, independent claim 19 defines that the speed of the computation unit is inversely proportional to the variable (temperature or charge) of an electrical capacitor, by which the state of the state unit can be represented. However, and inverse proportionality is a very well defined relationship, which comprises more information than just indicating "when the temperature decreases, the frequency increases". Rather, an inverse proportionality clearly defines that a doubling of the variable (temperature or charge) results in a reduction of the speed by a factor of 2. Such a relationship is not disclosed in Curiger. Also, Curiger does not disclose any inversely exponential relationship between a state variable and a speed of computation.

Thus, the subject matter of new independent claim 22 should be considered allowable.

Regarding new independent claim 23, Curiger does not show a step-wise change of a speed of a computation unit in dependence on the state of a state unit. Regarding the on chip oscillator, Curiger describes that the frequency of the on chip oscillator is affected by temperature. However, this relationship is clearly a continuous relationship, not a step-wise relationship. Moreover, Curiger describes that a temperature sensing circuitry will initiate a reset and hold the chip in reset until a temperature falls below the maximum operating temperature. However, resetting the chip is not related to the on chip oscillator. In contrast, the frequency of the on chip oscillator will merely be affected by the continuous temperature impact, but will not

change in steps. In other words, Curiger is silent about two different discrete speed values, namely a first high speed and a second lower speed.

Regarding new independent claim 24, Curiger is completely silent about any mechanism for adjusting a relationship between a state of a state unit and a speed of the calculation unit making use of a programmable parameter. Rather, the relationship between the frequency of the on chip oscillator according to Curiger and the temperature of the chip is a predetermined fixed relationship which is determined by the circuit design. In other words, predetermined design parameter and uncontrollable process variances determine the speed of the oscillation circuit according to Curiger. In contrast, the present invention as defined by the new independent claim 24 makes use of programmable parameters, e.g. multi-implicative factors, which can be set by a software developer, who designs the program for the processor.

In other words, while all the parameters of the on chip oscillator are fixed by the hardware design according to Curiger, the present invention allows for a programmable (e.g. software based) definition of a relationship between the state of the state unit and the speed of the calculation unit.

Regarding new independent claim 25, Curiger is silent about adjusting a number of bits which are processed simultaneously according to a state of a state unit, when the state of the state unit is increased in response to the execution of an operation by the computation unit.

Regarding new independent claim 26, Curiger is completely silent about introducing wait clock intervals in order to decrease the speed of a calculation unit in response to the execution of an operation by the computation unit.

In summary, neither Curiger nor any other reference, whether taken alone or in any combination, either shows or suggest the features of any of the claims as presented above. The amended claims are believed to be patentable over the prior art of record.

In view of the foregoing, reconsideration and allowance of claims 1-6 and 10-26 are solicited.

Counsel's payment in the amount of $ 1550.00 for three extra claims over 20 and seven extra independent claims is submitted herewith. Please charge any additional fees which may be due to deposit account No. 12-1099 of Lerner Greenberg Stemer LLP.

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WHS:lq

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